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Formation of inversion layers in organic field-effect transistors

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An inversion current in unipolar organic field-effect transistors is not observed, which can be due to trapping of electrons or to negligible electron injection. Here, we distinguish between both cases by studying the depletion current of unipolar *p*-type transistors based on a deliberately doped organic semiconductor. For each doping level, the current can be completely pinched off, which unambiguously shows that no inversion layer is formed. Numerical calculations show that for electron injection barriers >1 eV, the transistor is thermodynamically not in equilibrium, such that a steady state is not reached in the time frame of the experiment.

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I. INTRODUCTION

Organic field-effect transistors (OFETs) are being investigated for their use in high-volume applications such as radio-frequency identification tags, pixel engines in active matrix displays, and sensors.¹⁻⁴ In silicon-based electronic circuits, complementary metal-oxide-semiconductor (CMOS) logic is applied, for which both *p*-type and *n*-type transistors are required. The advantages over unipolar logic are low power dissipation and robust operation.⁵ In contrast to silicon many organic semiconductors are unipolar, in the sense that the hole conduction is significantly larger than the electron conduction. The electron current is reduced by traps, with typically densities of about 10^{17} cm⁻³.⁶ As a result, most organic transistors are normally ON unipolar *p*-type transistors. Holes are accumulated at negative gate bias, resulting in an accumulation current between the source and drain electrode. At positive gate bias, however, the measured current is negligible. Holes in the semiconductor are depleted, eliminating the hole current. Because the total current is the sum of the electron and hole current, the electron current is also negligible.

The absence of an electron current is remarkable: theoretically, semiconductor physics predicts in steady state both depletion of holes and inversion, i.e., accumulation of electrons at the semiconductor-dielectric interface. Inversion should always occur because the formation of a negatively charged layer at the semiconductor/insulator interface that screens the electric field of the positively biased gate electrode is energetically the most favorable situation. The fundamental question arises whether the absence of electron current in OFETs is due to trapping of electrons or to the fact that the steady state is not reached. In the first scenario electrons are injected from the contacts but are immobilized either in the bulk of the semiconductor or at the semiconductor-dielectric interface. Trapping in the bulk of the semiconductor is unlikely, because the charge-carrier densities in OFETs are in the range of 10^{19} cm⁻³, two orders of magnitude higher than the bulk electron trap density. Therefore, at these densities all the bulk electron traps are filled and do not play a role in the transport. However, it has been demonstrated by Chua *et al.* that also severe trapping of electrons at the semiconductor

occurs, due to the presence of hydroxyl groups.⁷ As a result, the electron current is negligible, regardless of the electron mobility in the bulk. In the second case the rate of electron injection and generation is too low. Many OFETs make use of Au source and drain contacts, which, because of their high work function, are good hole injectors, but poor electron injectors. The very large injection barriers do not supply the amount of electrons required to form an inversion layer. The steady state is not reached within the time scale of the dc measurements. The electron current, then, is negligible because the inversion channel has not been formed yet.

Here, we distinguish between both cases using unipolar *p*-type transistors, based on a deliberately doped organic semiconductor. By doping the semiconductor, mobile holes are induced, resulting in a measurable bulk current. A positive applied gate bias depletes the holes from the semiconductor. However, if inversion sets in, the gate bias is screened by the (trapped) electrons at the interface. Further increase of the gate bias results in stronger inversion but not in further depletion of the bulk of the semiconductor. Full depletion of the bulk is only possible if the gate bias is not screened by an inversion layer. Hence the occurrence of an inversion layer, formed by either mobile or trapped electrons at the semiconductor-dielectric interface, can be inferred from the observation of the depletion current at positive gate bias. Numerical two-dimensional (2D) charge transport simulations were used to calculate the electron and hole distributions without making *a priori* assumptions on the profiles. The screening dynamics can artificially be introduced by either including or suppressing electrons in the software.

II. RESULTS AND DISCUSSION

Transistors with a bottom-gate bottom-contact configuration were fabricated as described previously.⁸ As a semiconductor, regioregular poly(3-hexylthiophene) (P3HT) was selected to allow comparison of electrical transport with literature reports.^{8,9} The experimental details are presented in the Appendix. At negative gate bias, holes are accumulated and form a *p*-type conducting channel. Linear transfer curves measured as a function of temperature are presented in Fig. 1. The current increases both with increasing temperature and

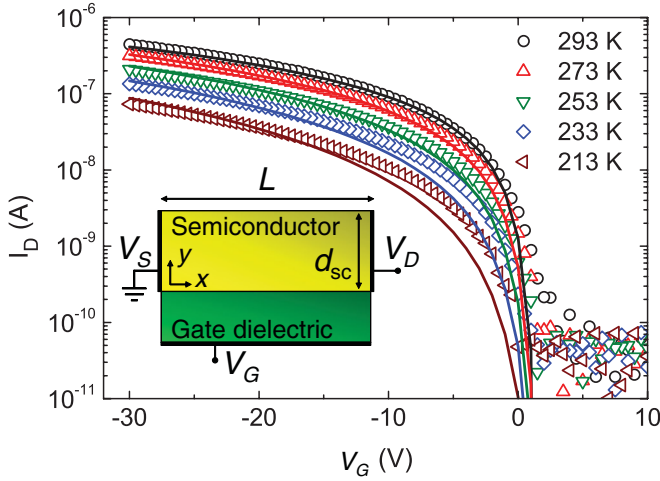


FIG. 1. (Color online) Linear transfer curves of a P3HT transistor as a function of temperature and measured at a drain bias of -2 V. Experimental data are represented by symbols and the numerical simulations by solid lines. The channel width and length are 1000 and 40 μm . The inset shows a schematic representation of a bottom-gate bottom-contact transistor.

gate bias. No current is measured for positive gate bias. The transfer curves were modeled numerically. To calculate the current, a mesh was defined, and at each point Poisson's equation, the continuity equations and the drift-diffusion equations were iteratively solved.^{10–12} Electrical conduction in organic semiconductors occurs by thermally activated hopping of charge carriers between localized states. Here, we approximate the density of localized states (DOS) by an exponential DOS.¹³ The local mobility then increases as a power law with charge-carrier density. Details on the numerical modeling are presented in the Appendix. The only fit constants to calculate the current are the parameters describing the hole mobility as a function of charge-carrier density and temperature. The solid lines in Fig. 1 show that with values rather similar to previously reported numbers,⁸ a good agreement is obtained.

For positive bias, the numerical calculations do predict inversion in the steady state.¹⁴ However, the calculated electron currents are below the experimental detection limit. The low current is due to the contact definition; the boundary conditions for the contacts strongly influence the calculated current. The highest occupied molecular orbital (HOMO) of P3HT aligns well with the work function of Au forming an ohmic contact for holes. We assume thermionic emission, resulting in a high hole density at the contacts.^{15,16} As a consequence, the injection barrier for electrons is approximately equal to the band gap. The corresponding electron density at the contact is very low, leading to low electron currents, even in the presence of an inversion layer. As a result from undoped semiconductors with ohmic hole contacts, it can experimentally not be verified whether an inversion layer is formed or not.

To address this question, we studied the charge transport in deliberately doped semiconductors by using oxidizing agents. By doping the semiconductor, mobile holes are induced yielding a bulk current at zero gate bias. Application of a positive gate bias depletes the semiconductor of holes to a

depth dependent on the gate bias and the doping density.¹⁴ When the depletion depth is larger than the semiconductor layer thickness, the bulk current is completely pinched off. At positive gate bias, when holes are depleted, electrons might be accumulated at the semiconductor-dielectric interface. When such an inversion layer is formed, the accumulated electrons screen the gate potential. A further increase of the gate bias then does not further deplete the bulk semiconductor but leads to an additional accumulation of electrons. The maximum depletion depth of the semiconductor, $d_{\text{depl,max}}$, is given by¹⁴

$$d_{\text{depl,max}} = \lambda_D \sqrt{4 \ln(N_A/n_i)} \text{ with } \lambda_D = \sqrt{\frac{\epsilon_0 \epsilon_{\text{sc}} k_B T}{e^2 N_A}}, \quad (1)$$

where λ_D is the Debye length, a characteristic length for charge screening in semiconductors and n_i is the intrinsic carrier density. If the semiconducting layer thickness is larger than the maximum depletion depth, a doped region remains. As a result, a finite bulk current remains, indirectly indicating the presence of an inversion layer. We note that the screening length is independent of the electron mobility. Hence, even when all electrons are trapped, a finite bulk hole current is expected. In case no inversion layer is formed, there are no electrons present to screen the gate bias. An increasing positive gate bias, then, further depletes the semiconductor, and the current is completely pinched off.

Here we dope a semiconductor *in situ* by exposing the transistor to a vapor of trichloro(1*H*,1*H*,2*H*,2*H*-perfluorooctyl)silane (TCFOS). It has been reported that the doping level in P3HT can be varied deliberately by changing the exposure time.^{17–19} The acceptor density ranges between 10^{16} – 10^{17} cm^{-3} and n_i is about 1.6×10^4 cm^{-3} , leading to a predicted maximum depletion depth between 40 and 200 nm. A semiconductor layer thickness of more than 200 nm was chosen, larger than the predicted maximum depletion depth. Linear transfer curves as a function of exposure time are presented in Fig. 2(a). With increasing exposure time, the transfer curves shift towards positive gate bias, and a shoulder appears in the subthreshold region. There is hardly any hysteresis. Gate bias stress can be disregarded on the timescale of the experiment. Each transfer curve represents a single doping level. We stress that for each doping level, the current can be completely pinched off. At high doping levels, the semiconductor layer thickness is larger than the predicted maximum depletion depth. The current in depletion being completely pinched off, therefore, unambiguously shows that no inversion layer is formed. There are no electrons at the semiconductor-dielectric interface to screen the gate potential.

To elucidate the absence of an inversion layer, we numerically calculated the transfer characteristics. The determination of the doping density follows a previously reported procedure²⁰ and is discussed in the Appendix. The calculated steady-state currents are presented as solid lines in Fig. 2(b). In accumulation a good agreement is obtained. In depletion, however, a gate-independent bulk current is calculated contrary to the experimental currents in Fig. 2(a). The reason is that in the steady state an inversion layer is calculated that screens the gate potential and thereby prevents full depletion of the bulk semiconductor. We have calculated the transfer curves by artificially suppressing the electron density

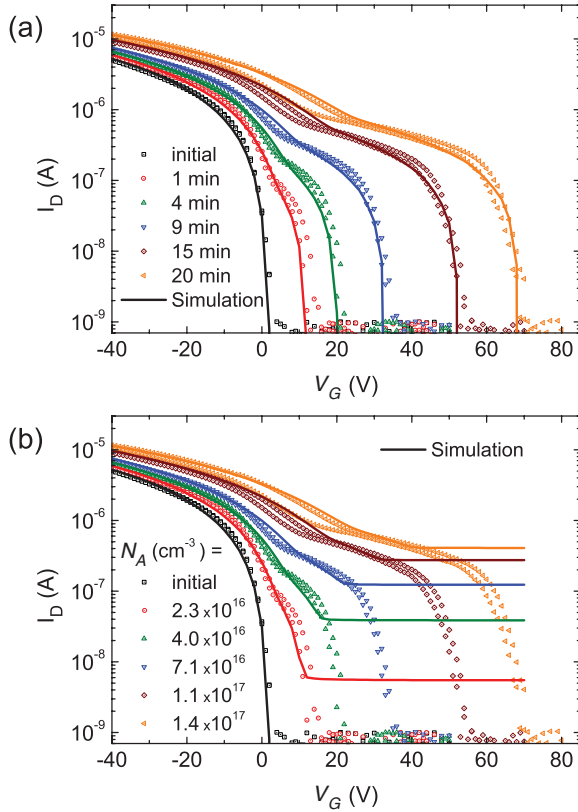


FIG. 2. (Color online) Linear transfer curves of a P3HT transistor doped with TCFOS as a function of exposure time, measured at a drain bias of -2 V. The P3HT film thickness was 205 nm, and the channel width and length were 2500 and 10 μm . (a) Measurements (symbols) and numerical calculations (lines) in which the electron density was artificially suppressed. (b) The same experimental data as in (a). The solid lines are numerical steady-state calculations.

in the whole device. All other parameters remain the same. The calculated currents are presented as the solid lines in Fig. 2(a). A good agreement is obtained, which demonstrates that experimentally no inversion layer is formed.

The steady-state densities for holes, electrons, and acceptors in the semiconductor are presented in Fig. 3(a), as a function of the distance from the semiconductor-dielectric interface. The densities are calculated in deep depletion. The semiconductor is heavily doped, corresponding to the blue curves (medium gray) in Fig. 2. The electron density [red line (dark gray)] is high at the semiconductor-dielectric interface and negligible further down in the semiconductor, forming a clear inversion layer. The hole density [blue line (medium gray)] is negligible at the semiconductor-dielectric interface and reaches further down in the semiconductor the bulk value, forming a depletion region for holes. The depletion width agrees with the calculated maximum depletion width using Eq. (1), as indicated by the dashed line in Fig. 3(a). The net charge in the semiconductor is given by $\rho = e(p - n - N_A)$, and presented in the lower part of Fig. 3(a). In the bulk there is no net charge; the gate bias is compensated for by the electrons and ionized acceptors in the depletion region. We note that upon increasing the gate bias in steady state, the depletion width does not change. The

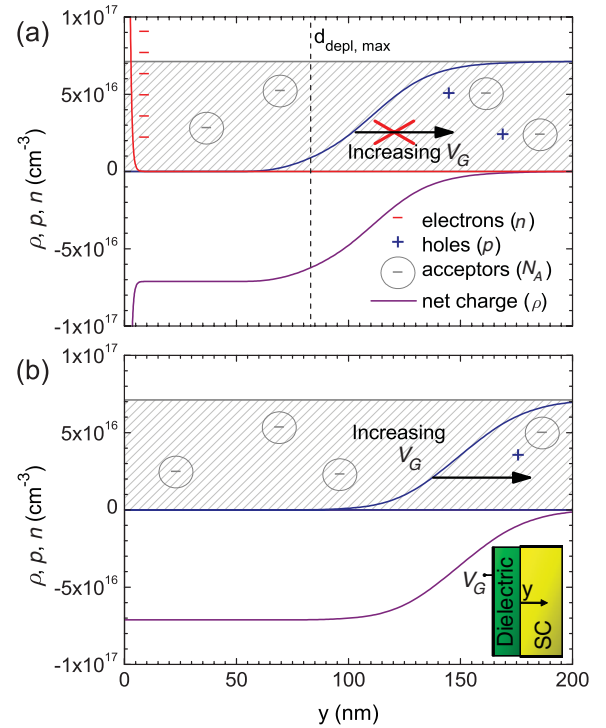


FIG. 3. (Color online) Calculated charge density in the semiconductor as a function of the distance from the semiconductor-dielectric interface, in the middle of the transistor channel. The acceptor density was $7.1 \times 10^{16} \text{ cm}^{-3}$. A gate bias of $+25$ V was applied to deplete the semiconductor from holes. (a) Steady-state calculations. The predicted maximum depletion width is indicated by the dashed line. (b) Electrons are artificially suppressed; the semiconductor is depleted as a function of the gate bias. The y direction is indicated in the schematic inset.

additional gate bias is fully compensated for by a concomitant increase in accumulated electrons. In Fig. 3(b), the charge profiles in the semiconductor are presented where the electrons were suppressed. The doping concentration and gate bias are identical to those of Fig. 3(a). No inversion layer is formed, and a larger part of the semiconductor is depleted. The calculated depletion width increases with gate bias. Experimentally, there is a large barrier for minority-carrier injection. It takes time to form an inversion channel. Hence, suppressing the electron density in the calculations corresponds to a transistor that is thermodynamically not in equilibrium. The good agreement between measured and calculated transfer curves indicates that the steady state is not reached.

The minority carriers, here electrons, in the channel can be delivered either by the contacts or by the bulk semiconductor.²¹ For standard silicon at room temperature, the minority-carrier response time is determined by generation and is in the order of 0.01 – 1 s. Silicon transistors operate at gigahertz frequencies because the minority carriers can be injected from the source and drain regions, which are heavily doped and in close contact to the channel.²² The generation rate has been estimated for organic semiconductors as a function of the band gap.^{22,23} The electron generation time in the bulk semiconductor and dielectric relaxation time corresponding to the transport of electrons to the channel both increase exponentially with the

band gap. The fastest process dominates the dynamic behavior. For a band gap of 2 eV, a response time of more than 10^6 s has been calculated.²² Hence, the supply of electrons from the bulk semiconductor can be disregarded.

In order to form an inversion layer, the carriers have to be supplied by the electrodes. The injection time is estimated from the total accumulated charge density and the injection current that can be delivered by the contact. The accumulation charge is approximated by $V_G C_i$, resulting in 10^{12} electrons/cm² at a typical gate bias of 10 V. For a transistor with a length and width of 10 and 2500 μm , the charge to be injected amounts to 4.3×10^{-11} C. We calculate the injection current as a function of injection barrier, which is the difference in work function of the electrode and the lowest unoccupied molecular orbital (LUMO) energy of the semiconductor. We take as the injection mechanism thermionic emission with image force lowering of the barrier, and two reported diffusion limited injection models.^{14,24} The calculated injection times as a function of injection barrier are presented in Fig. 4. The injected current and, hence, the injection time depend exponentially on the injection barrier. Therefore, in Fig. 4 straight lines are obtained. The injection barrier for P3HT and Au is about 1.7 eV. Figure 4 shows that the injection time is at least 10^8 s. The value is much larger than realistic measurement times, showing that the transistor is not in thermodynamic equilibrium. We note that in ambipolar transistors, which conduct both electrons and holes, the injection barriers are typically 1 eV or less. The calculated equilibrium times are less than 1 s, which confirms that both electrons and holes can indeed be supplied by the contacts within the experimental measurement time. Similarly, it should be noted that when electron-injecting source-drain contacts such as Ca or Ba are applied, the inversion layer will be formed in the time frame of the experiments, in agreement with the observations of Chua *et al.*⁷ In that case the barrier for hole injection will be large such that the formation of the

hole accumulation layer at negative gate bias will be strongly hampered.

III. SUMMARY

In summary, we have studied the formation of an inversion layer in organic normally ON unipolar *p*-type transistors. At positive gate bias the measured current is negligible. The absence of the electron current can either be due to trapping or to the fact that the steady state is not reached. By studying the depletion current of unipolar *p*-type transistors based on a deliberately doped organic semiconductor, we can disentangle these mechanisms because an inversion layer screens the gate bias. Numerically calculated steady-state currents show in accumulation a good agreement with experimental currents. In depletion, agreement could only be obtained by suppressing the electron density, which demonstrates that experimentally no inversion layer is formed. In order to form an inversion layer, the carriers have to be supplied by the electrodes. We estimate the injection time assuming thermionic emission or diffusion-limited injection models as the injection mechanism. For a barrier of 1.7 eV, we arrive at an injection time of at least 10^8 s. Hence, an inversion layer is not formed because the transistors are not in thermodynamic equilibrium, and the steady state is not reached.

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APPENDIX

1. Numerical device model

The electrical transport is governed by Poisson's equation, the continuity equations, and the drift-diffusion equations. Poisson's equation relates the local potential to the charge density

$$-\epsilon_0 \epsilon_{sc} \nabla^2 \psi = e(p - n + N_D - N_A), \quad (\text{A1})$$

where ψ is the electrostatic potential and p and n are the hole and electron densities. N_D and N_A are the ionized donor and acceptor densities, which induce doping, ϵ_0 is the vacuum permittivity, ϵ_{sc} is the relative permittivity of the semiconductor, and e is the elementary charge. The electron and hole density can vary with time due to recombination or due to a gradient in the current. The changes are expressed in the continuity equations as

$$e \frac{\partial p}{\partial t} = -\nabla J_p - eR, \quad (\text{A2a})$$

$$e \frac{\partial n}{\partial t} = \nabla J_n - eR, \quad (\text{A2b})$$

where J_p and J_n are the local hole and electron current density and R the Langevin recombination rate. The current densities

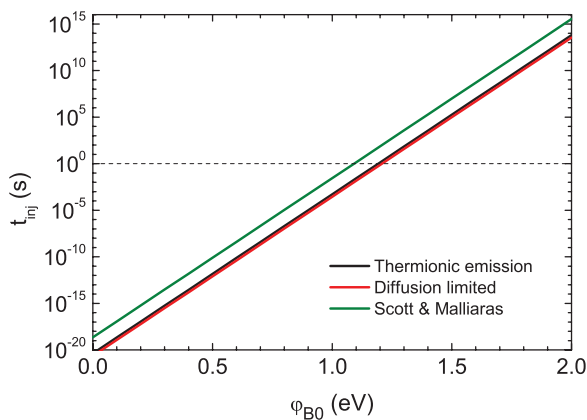


FIG. 4. (Color online) The time required to inject the steady-state charge in a field-effect transistor, calculated using three injection models. The calculations are based on a transistor with a width, length, and height of 2500 μm , 10 μm , and 205 nm and a gate bias of 10 V. The value for the Richardson constant was estimated as $100 \text{ A K}^{-2} \text{ T}^{-2}$ (Si), the mobility was $0.01 \text{ cm}^2/\text{V s}$, the electric field at the injecting contact was $5 \times 10^6 \text{ V/cm}$, and the density of states of the valence band was $N_V = 2 \times 10^{21} \text{ cm}^{-3}$. The dashed line indicates the time scale of the measurement.

depend on the local electric field and gradients in the density of holes and electrons. The corresponding drift-diffusion currents for holes and electrons then follow from

$$J_p = e\mu_p \left(pE - \frac{k_B T}{e} \nabla p \right), \quad (\text{A3a})$$

$$J_n = e\mu_n \left(nE + \frac{k_B T}{e} \nabla n \right), \quad (\text{A3b})$$

where μ_p and μ_n are the hole and electron mobilities, k_B is the Boltzmann constant, T is the temperature, and E is the electric field. The electric field is the gradient of the electrostatic potential, implying that Eqs. (A1)–(A3) are coupled. They can be solved self-consistently yielding locally p , n , and ψ . To find the current in a transistor, coupled to the solution for p , n , and ψ , the device has to be divided in discrete points. A steady-state solution can be found iteratively, for instance, using the Newton method.¹⁰ An expression for the mobility is required, and boundary conditions for the contacts have to be imposed.

Contrary to typical inorganic semiconductors, the charge-carrier mobility in organic semiconductors depends on the charge-carrier density. Various temperature, density, and field-dependent mobility models have been reported.^{13,25–30} Here, we assume that charge transport is described by variable range hopping in an exponential DOS.¹³ The hole mobility then reads

$$\mu_p = f(T)p^{T_{\text{rel}}-1}, \quad (\text{A4a})$$

with a temperature-dependent prefactor given by

$$f = \frac{\sigma_0}{e} \left[\frac{T_{\text{rel}}^4 \sin\left(\frac{\pi}{T_{\text{rel}}}\right)}{(2\alpha)^3 B_C} \right]^{T_{\text{rel}}}, \quad (\text{A4b})$$

where σ_0 is a conductivity prefactor, α^{-1} is an effective overlap parameter, and B_C is related to the onset of percolation and given by 2.8 for three-dimensional systems. $T_{\text{rel}} = T_0/T$, where T_0 is a characteristic parameter describing the width of the density of states. A similar expression holds for electrons.

The boundary conditions strongly influence the calculated current. A detailed description of the charge injection is beyond the scope of this work. Here, we assume thermionic emission with ohmic contacts for holes, resulting in a high hole density at the contacts.^{15,16} As a consequence, the injection barrier for electrons is approximately equal to the band gap.

Software packages to numerically calculate electrical transport in microelectronic devices are commercially available. Most packages are designed for conventional crystalline semiconductors, i.e., the underlying physics is based on band transport. For accurate simulations of organic semiconductors, a software package is required in which a charge-carrier-dependent mobility, any injection model, and bulk doping can easily be implemented.^{15,16,31–33} Here we used the CURRY package, previously developed at Philips Research, because it offers the required flexibility to implement user-defined functions.^{10–12,34}

The bottom-gate bottom-contact transistor layout is presented in the inset of Fig. 1. The transistor channel length is indicated by L , and the semiconductor thickness by d_{sc} . The width, W , of the transistor is much larger than the length. Hence, transport along the width can be assumed to be uniform, allowing for 2D simulations. A rectangular mesh was used

to map the transistor. Perpendicular to the gate, the mesh spacing in the semiconductor was several nanometers. To accurately calculate the large gradient in carrier density close to the gate-dielectric interface, the spacing in this region was exponentially reduced to 0.01 nm at the interface. In the lateral direction the mesh lines had a spacing of 250 nm. Close to the source and drain contacts, the spacing was exponentially reduced to 2 nm.

To account for interface charge density, Q_i , at the semiconductor-dielectric interface causing a shift of the switch-on voltage, V_{SO} , a thin layer with a fixed space charge density was defined in the dielectric at the interface. The charge density in this layer was calculated by Q_i/d , where d is the thickness of the charged layer, chosen to be 1 nm. To describe a doped semiconductor, a uniform acceptor doping density was assigned to the semiconductor layer. The dielectric constants used in the calculations were 3.9 for SiO_2 , and 3 for P3HT.

To artificially suppress the electron density in the calculations as described in the text, the quasi-Fermi level for electrons, φ_n , was adjusted. In steady-state calculations, φ_n is solved. To prevent the steady state, we manually fixed φ_n at an arbitrarily high value of 500 V. The electron density is then negligible, as it follows from the Boltzmann relation, given by

$$n = n_i \exp\left(\frac{e(\psi - \varphi_n)}{k_B T}\right) \quad \text{with} \quad n_i = N_V \exp\left(\frac{-E_g}{2k_B T}\right), \quad (\text{A5})$$

where n_i is the intrinsic carrier density, E_g is the band gap, and N_V is the effective density of states of the valence band and taken as $N_V = 2 \times 10^{21} \text{ cm}^{-3}$. For a typical band gap of 2 eV, n_i is about $1.6 \times 10^4 \text{ cm}^{-3}$ at 295 K.

2. Device fabrication and characterization

Transistor test substrates were fabricated on a heavily n -doped silicon wafer acting as a common gate electrode. Thermally grown SiO_2 passivated with hexamethyldisilazane (HMDS) was used as the gate dielectric. Au source and drain electrodes were defined using conventional photolithography, using Ti (10 nm) as an adhesion layer. To minimize the influence of short-channel effects and contact resistances, channel lengths larger than 10 μm were used.

For a polymeric semiconductor, P3HT was used. P3HT was spin cast in an N_2 atmosphere from chloroform (10–20 mg/ml), and the transistors were subsequently annealed in a vacuum oven at 150 °C for 2 h.

Transistors were doped by exposing them to a vapor of TCFOS (Sigma Aldrich). The measurement chamber was evacuated to less than 10^{-4} mbar. Then, 20–60 μl of TCFOS was injected into an antechamber. A valve to the measurement chamber was opened, resulting in a TCFOS partial pressure of 10^{-2} mbar. The transistors were measured as a function of exposure time.

Electrical characterization was performed in a dynamic vacuum ($<10^{-4}$ mbar) and in the dark. Measurements were performed using a Keithley 4200 Semiconductor Measurement System.

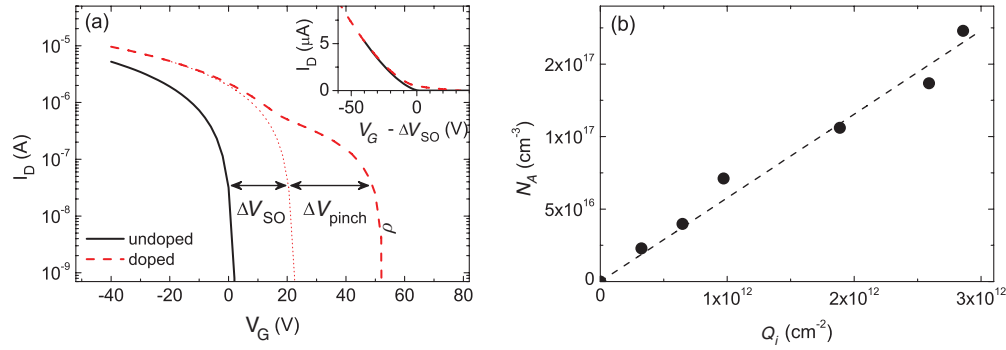


FIG. 5. (Color online) (a) Transfer curves of a P3HT field-effect transistor. The P3HT film thickness was 205 nm, and the channel width and length were 2500 and 10 μm . The transfer curves were measured in the linear regime at a source drain bias of -2 V before and after exposure to TCFOS. The figure shows the definition of ΔV_{SO} and ΔV_{pinch} . (b) The calculated bulk acceptor density N_A versus the surface charge-density Q_i .

3. Comparison with experimental results

The undoped P3HT transistor, presented in Fig. 1, was numerically simulated using the following mobility parameters: $\sigma_0 = 2.86 \times 10^6$ S/m, $T_0 = 350$ K, $\alpha^{-1} = 2.6$ Å, and $V_{\text{SO}} = 2$ V. The mobility determined at a gate bias of -30 V was 0.03 cm²/V s at room temperature, which is a typical value for P3HT.^{35,36} Because the mobility is temperature dependent, measurements at different temperatures are needed to correctly determine the parameters. The parameter set is unique; it is not possible to exchange σ_0 and α .

The doped P3HT transistor in Fig. 2 was simulated in several steps. First, the pristine situation was described using $\sigma_0 = 1.58 \times 10^7$ S/m, $T_0 = 371$ K, $\alpha^{-1} = 1.6$ Å, and $V_{\text{SO}} = 3$ V. The numbers were slightly different from those of the undoped transistor. The values are frozen in the calculations of the doped transistors. Next, the shift upon TCFOS exposure was modeled using both an acceptor doping level, N_A , in the semiconductor and an interface charge, Q_i , at the semiconductor-dielectric interface.

As shown in Fig. 5(a), the total shift of the transfer curve upon exposure to the TCFOS consists of two distinct voltage shifts: a shift of the switch-on voltage, ΔV_{SO} and of the

pinch-off voltage, ΔV_{pinch} . From ΔV_{pinch} the acceptor dopant density can be derived as described previously.^{19,20} Assuming a uniform doping profile, N_A follows from

$$N_A = \frac{\Delta V_{\text{pinch}}}{ed_{\text{sc}} \left(\frac{d_{\text{sc}}}{2\epsilon_0\epsilon_{\text{sc}}} + \frac{1}{C_i} \right)}, \quad (\text{A6})$$

where d_{sc} is the semiconductor thickness and C_i is the gate capacitance per unit area. The switch-on voltage, V_{SO} , is modeled by introduction of an interface charge density as $Q_i = -(V_{\text{SO}} + \Delta V_{\text{SO}}) C_i/e$. Figure 5(b) shows that Q_i scales linearly with N_A . This relation can be expected because TCFOS oxidizes the semiconductor, changing N_A , as well as the interface states, changing Q_i . The ratio depends on the surface coverage of the HMDS.

In the calculations of the doped transistor, a single expression for the charge-dependent mobility was used. The good fits indicate that the bulk mobility and channel mobility have the same functional charge-density dependence. This is in contrast with previously reported semiconductor-dopant systems,^{20,37,38} in which the bulk mobility was found to depend much stronger on density than the channel mobility.

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